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10041601  
01/10/02

PATENT NUMBER and  
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10041601	FILING DATE 01/10/2002	CLASS 357	SUBCLASS /	GAU 2018 2015	EXAMINER <i>YDIA</i>
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\*\*CONTINUING DATA VERIFIED: *TN*

\*\* FOREIGN APPLICATIONS VERIFIED:

JAPAN 2001-010787 01/18/2001 *TN*

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>	ATTORNEY DOCKET NO
Foreign priority claimed 35 USC 119 conditions met Verified and Acknowledged Examiners's initials		<input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input checked="" type="checkbox"/> yes <input type="checkbox"/> no	<i>TN</i> XA-9596
TITLE : Semiconductor integrated circuit device			
U.S. DEPT. OF COMM./PAT. & TM-PTO-436I (Rev. 12-94)			

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G.
ISSUE FEE		DRAWING		
Amount Due	Date Paid	Sheets Drwg.	Figs.Drwg.	Print Fig.
TERMINAL DISCLAIMER		Primary Examiner		
		Application Examiner		
PREPARED FOR ISSUE				
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